Low-Cost and TSV-free Monolithic 3D-IC with Heterogeneous Integration of Logic, Memory and Sensor Analogy Circuitry for Internet of Things

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Abstract

For the first time, a CO2 far-infrared laser annealing (CO2-FIR-LA) technology was developed as the activation solution to enable highly heterogeneous integration without causing device degradation for TSV-free monolithic 3DIC. This process is capable to implement small-area-small-load vertical connectors, gate-first high-k/metal gate MOSFETs and non-Al metal inter-connects. Such a far-infrared laser annealing exhibits excellent selective activation capability that enables performance-enhanced stacked sub-40nm UTB-MOSFETs (Ion-enhanced over 50 %). Unlike TSV-based 3D-IC, this 3D Monolithic IC enables ultra-wide-IO connections between layers to achieve high bandwidth with less power consumption. A test chip with logic circuits, 6T SRAM, ReRAM, sense amplifiers, analog amplifiers and gas sensors was integrated to confirm the superiority in heterogeneous integration of proposed CO2-FIR-LA technology. This chip demonstrates the most variable functions above reported 3D Monolithic ICs. This CO2-FIR-LA based TSV-free 3D Monolithic IC can realize low cost, small footprint, and highly heterogeneous integration for Internet of Things.

I. Introduction:

Driven by growing demand for Internets of things (IoT), IC technology requires continuous innovations for low-power consumption, and multi-function IoT chips using low cost fabrication process [1-2]. Thus, TSV-free monolithic three dimensional integrated circuits (3D-IC) exhibits the advantages of (1) cost-effective manufacturing (2) small area and low parasitic load for vertical signal communications, and (3) highly heterogeneous integration capability [3-7], including logic, memory, analog, sensors and energy harvesters (Fig. 1a). One of the main challenges of the TSV-free monolithic 3DIC is how to effectively activate FET junction at the upper-layers using low thermal budget technology to prevent degradation of pre-existing devices. In this work, compromised low temperature annealing process (~600 °C) (beyond back-end process temperature) or UV-visible laser activation (metal-gate and interconnect damage issue) [3-5] was replaced by low thermal budget CO2 far-infrared (λ=10.6µm) laser activation (400 °C) which enables effective activation strictly confined at source/drain region by defect-related free carrier absorption and no damage on metal gate and non-Al interconnects due to intrinsic high reflection of far-infrared light. Stackable channel layers were enabled by super-CMP-planarized and visible laser-crystallized epi-like Si channel technology as a low cost solution for monolithic 3D-IC. Over 50 % Ion-enhancement in stackable sub-40nm UTB-MOSFETs was achieved using CO2-FIR-LA. A test chip with logic circuits, 6T SRAM, ReRAM, sense amplifiers, analog amplifiers and gas sensors was integrated to confirm the superiority in heterogeneous integration of the proposed CO2-FIR-LA technology.

II. Device Fabrication:

In sequentially processed sub-40nm monolithic 3D-IC with stackable Si UTB n/p MOSFETs, SRAM array and core peripherals circuits as well as sensor analog circuitry were fabricated using stackable low cost epi-like Si channel, plasma-ALD (Syskey Technology LTD.) HfO2/TaN high-k metal-gate and CO2 laser (Coherent Inc.) activation (Fig. 1b). Low temperature ReRAM and gas sensor were fabricated for the hetero-integrated IoT Chips.

III. Results and Discussion:

(A) CO2-FIR-LA stackable UTB-MOSFETs and 6T-SRAM array:

Fig. 2 shows the performance improvement of stackable Si UTB n/p MOSFETs using CO2 laser activation technology with on-currents as high as 216/178 μA/μm (|Vd|=1V) and
steep sub-threshold slope of 88/92 mV/dec, compared with previous IEDM 2014 results [8] using microwave/visible laser annealing technology. After upper-layer CO$_2$-FIR-LA process (Fig. 3a), no laser damage on existing 0.18 μm non-Al metal interconnects (Fig. 3b) and 6T-SRAM (Fig. 3c) were confirmed. Fig. 4 presents the schematic and photo of 6T SRAM. Thanks to the modification of HK/MG engineering and activation technology, the 6T SRAM achieved 150 mV in hold-SNM at supply voltage (VDD) = 0.5V. This experiment also confirms the read/write operation across various VDD (1.0V, 0.7V and 0.5V).

(B) Function confirmation for decoder, sense amplifier, level shifter and ReRAM: In this work, we have further developed the peripheral circuits for memory beyond previous works [8-11], including logic (decoders) and sense amplifier, as Fig. 5 and Table 1 shown. The measured waveform (Fig. 5d) confirms the logic function of a 3-to-8 decoder. Fig. 6 presents the schematic and photo of implemented voltage-mode sense amplifier (SA). Fig. 6(e) shows the measured waveform confirms the function of a sense amplifier with 100 mV differential input. Fig. 7 shows the schematic and photo of the level-shifter for non-volatile memory (NVM) usage, such as ReRAM in this work. The measured waveform in Fig. 7(e) confirms that the level-shifter can convert a low input voltage (0.7V) to the higher voltages (2.6V) required for the SET/RESET operation of ReRAM (Fig.8).

c) Analog circuit and sensor: This work also implements a pre-amplifier for sensors to demonstrate analogy circuitry in our 3D-IC process (Fig. 9). The two-stage pre-amplifier consists of a differential pair, and a single-ended rail-to-rail output stage. The unit gain bandwidth (GBW) is a few kHz providing sufficient gain for most IoT sensors, such as heart beat, acceleration, voice, light and gas sensing applications. In this work, a carbon monoxide (CO) gas sensor with enhanced performance by using Au nanoparticles is implemented, as shown in Fig. 10.

IV. Conclusion: Laser annealed TSV-free 3D-IC with heterogeneous integration of logic, memory and sensor analogy circuitry was demonstrated. This CO$_2$-FIR-LA based TSV-free monolithic 3D-IC can realize low cost, compact area and highly hetero-integrated 3D chips for Internet of Things.

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References:
This work, using CO2-FIR-LA | IDMS 2014, our group

0.18 μm W-plug

W-feature size 0.5, 0.5, 0.18 μm

Current (mA) Voltage (V)

Dash line: before CO2-FIR-LA
Solid line: after CO2-FIR-LA

500 nm ILD

a-Si deposition

Laser crystallization
GN-LA, λ = 532 nm

CMP (channel thinning)
E-beam litho. (active area)
Chemical SiO2
ALD HfO2 gate oxide
TaN gate
E-beam litho. (gate length)
S/D implantation (BF2/As)
Laser activation
CO2-FIR-LA, λ = 10.6 μm

Self-aligned silicide

Metallization

Low Cost Epi-like Si Channel
GN-LC

CO2-FIR-LA

Low Thermal Budget CO2-FIR-LA

After upper layer CO2-FIR-LA

VDD=1.0V

B
C
A( = 1 )

D0
D1

1     1    1    1
0 1    1    0
1     1 0    0
00 1 0
1 0    0    0

VDD = 1.0 V

(d)

0.7V and 0.5V.

SRAM Array

Sensor

Ambient Light

Energy Harvester

Wide IO

Micro Control Unit

ReRAM Array

SRAM Array

Decoder

RAM Array

Decomposer

Analog Start

Fig. 1. (a) Conceptual illustration of monolithic 3D-IC with MCU, analog circuits, memories for Internet of Things. (b) Process flow for TSV-free monolithic 3DIC using low cost epi-like channel and CO2 far-infrared laser annealing (CO2-FIR-LA) technology.

1. Top Tier MOSFETs -> CO2-FIR-LA at S/D (no damage on metal gate)
2. Existing Circuits -> Higher Laser Light Reflection (no damage to BEoL & FEoL)
3. Existing Si Channels -> Grain Boundary Defect Anneal (no damage)

Fig. 3. (a) Schematic of CO2 far-infrared laser activation damage test on metallization (back-end-of-line, BEoL) and circuit functional test (front-end-of-line, FEoL). No degradation was observed in both cases, (b) 0.18μm W metal-interconnect and (c) a 6T SRAM cell hold-SNM.

Fig. 4. (a) Photograph of a stackable 6T-SRAM array, (b) hold SNM, (c) read SNM and (d) write SNM of stackable 6T-SRAM at VDD = 1.0V, 0.7V and 0.5V.

Fig. 5. (a) Placement in a memory macro, (b) schematic circuit, (c) photograph, (d) measured results at VDD = 1.0V and (e) measured results with upper-layer CO2-FIR-LA at VDD = 1.0V for a 3-to-8 decoder. No laser damage was observed on existing decoder.
Fig. 10. (a) Au nanoparticles enhanced CO gas sensor is fabricated by stackable low thermal budget process, which includes trench structure, SiO2/SiNx, interdigitated electrode, micro-heater, and SnO2/Au nanoparticles. (b) The response of the sensing film upon exposure to CO gas injection and pumping.

Table I. Comparison of monolithic 3D-IC technology.