Co-Optimization of Signal, Power, and Thermal Distribution Networks for 3D ICs

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Abstract—Heat removal and power delivery are two major reliability concerns in the 3D stacked IC technology. Liquid cooling based on micro-fluidic channels is proposed as a viable solution to dramatically reduce the operating temperature of 3D ICs. In addition, designers use a highly complex hierarchical power distribution network in conjunction with decoupling capacitors to deliver currents. However, these thermal and power/ground interconnects together with those used for signal delivery compete with each other for routing resources including various types of Through-Silicon-Vias (TSVs). This paper presents the first work on routing with these multi-functional interconnects in 3D: signal, thermal, and power distribution networks. We demonstrate how to consider various physical, electrical, and thermo-mechanical requirements of these multi-functional interconnects to successfully complete routing while addressing various reliability concerns.

I. INTRODUCTION

It is widely accepted that three-dimensional (3D) system integration is a key enabling technology and has recently gained significant momentum in the semiconductor industry. However, there are a number of interconnect challenges that need to be addressed to enable stacking of high-performance dice, especially in the area of cooling. When two 100W/cm² microprocessors are stacked on top of each other, for example, the net power density becomes 200W/cm², which is beyond the heat removal limits of currently available air cooled heat sinks. Thus, cooling is the key limiter to stacking of high-performance chips today. This issue has recently been addressed with a novel 3D integration technology that features the use of a microchannel heat sink in each strata of the 3D system and the use of wafer-level batch fabricated electrical and fluidic chip input/output (I/O) interconnects [1].

Another major challenge is power delivery. As the fabrication technology advances, power consumption of the chip increases. As multiples chips are stacked together into a smaller footprint, delivering current to all parts of the 3D stack while meeting the noise constraints becomes highly challenging. This is mainly because the number of through-silicon-vias (TSVs) available for signal nets and P/G nets is limited, causing routing congestion if many 3D connections are desired. This issue is further exacerbated when micro-fluidic channels (and TSVs) are used for liquid cooling. Figure 1 shows a possible configuration of microfluidic channels and signal and P/G TSVs, all competing for layout resource.

We present the first work on routing with multi-functional interconnects—signal, power, thermal—in 3D ICs. We demonstrate how to consider various physical, electrical, and thermo-mechanical requirements of these multi-functional interconnects to successfully complete routing while addressing thermal and noise concerns. We demonstrate the effectiveness of our approach using large-scale gate-level benchmarks that contain up to 1.2 million gates. We report routing congestion, thermal distribution, and power supply noise based on full-layouts of 4-die 3D IC.

II. THERMO-FLUIDIC INTERCONNECT FOR 3D ICs

A. Fabrication of Microfluidic Channels and TSVs

Unlike air-cooled heat sinks, liquid cooling using microchannels offers a larger heat transfer coefficient (and thus lower convective thermal resistance) and chip-scale cooling solution. In [1], both electrical and fluidic TSVs and I/Os were demonstrated. The electrical interconnects are used for power delivery and signaling between strata, and the fluidic interconnects are used to deliver a coolant to each microchannel heat sink in the 3D stack and thus enable the rejection of heat from each stratum in the 3D stack. The chips are designed such that when they are stacked, each chip makes electrical and fluidic interconnection to the dice above and below. Consequently, power delivery and signaling can be supported by the electrical interconnects (solder bumps and copper TSVs), and heat removal for each stratum can be supported by the fluidic I/Os and microchannel heat sinks. The thermal resistance of the microchannel heat sink for single chip was previously measured [2]. When de-ionized water was used as coolant, the junction-to-ambient thermal resistance of the heat sink was 0.24°C/W at a flow-rate of about 65mL/min without TSVs (impact of copper TSVs on thermal conductivity of the silicon microchannel wall is negligible), which is significantly better than current state-of-the-art air cooled heat sinks [2]. The smallest resistance possible for air-cooled heat sink is around 0.5°C/W.

B. Routing Requirements for Thermo-fluidic Network

The on-chip thermo-fluidic network is composed of fluidic TSVs and microfluidic channels. In this work, we assume that all the fluidic TSVs are located outside the main region where all the gates and metal wirings are distributed. Thus, only the microfluidic channels are considered for routing requirement analysis. Since microfluidic channels are fabricated on the back side of a silicon die, they do

Fig. 1. A 3D die structure with microfluidic channels, power/ground TSVs, and signal TSVs. Transistors and signal wires are not shown for simplicity.
We first route the microfluidic channels, followed by the P/G TSVs on amount as discussed in Section IV-B. Some part of a P/G TSV, routing capacity is decreased by a large amount. TSV aspect ratio (AR, the ratio of the die thickness to the minimum TSV diameter) was assumed to be 15:1. Considering significant size of the microfluidic channels, they decrease the routing capacity of TSVs quite considerably. The scarce resource is usually the signal TSV capacity. Due to the microfluidic channels, many routing tiles have no capacity left for signal TSVs.

III. Power Delivery Network for 3D ICs

Overall power and ground structure is shown in Figure 2. In our work, power and ground (P/G) TSVs are placed regularly in a mesh structure with a predefined pitch ($P_{pg} = 400\mu m$). The width of a P/G tile is a half the power TSV pitch ($w_{pg, tile} = P_{pg}/2 = 200\mu m$) and contains one quarter of power TSV and one quarter of ground TSV. The total number of P/G TSVs in a die is:

$$N_{V_{pg}} = \left[ \frac{S_{chip}}{w_{pg, tile}^2} \right] \times (1/4 + 1/4)$$

where $S_{chip}$ is the area of the chip.

Power and ground nets are routed on metal layer 7 and 8. The following three-levels of wiring hierarchy is used:

- Thick wires have 10$\mu m$ width and runs between P/G TSVs.
- Between the thick wires, thin wires of 1$\mu m$ width and 4.64$\mu m$ pitch are placed.
- Between two thin wires, up to six signal wires can be routed.

In our 3D technology, two TSVs from two different dies are connected using the metal layers and vias in these dies. This means two stacked TSVs are not directly connected. In contrast, the diameter of P/G TSVs is assumed to be via-first. In via-first approach, TSVs are formed before metal wirings are constructed. From the signal routing point of view, this is beneficial because TSVs do not touch the metal interconnection layer. By contrast, in via-last approach, a TSV passes through the entire structure and decreases the metal wire interconnection space by a large amount. TSV aspect ratio (AR, the ratio of the die thickness to the minimum TSV diameter) was assumed to be 15:1.

Figure 3 shows the side view of a die. The diameter of signal TSVs is set to the minimum size to accommodate as many connections as possible. In contrast, the diameter of P/G TSVs is 40$\mu m$, which is comparable to our previous work [5]. Table II provides more details on related geometries. We fix the width of our routing tile $w_{r,tile} = 50\mu m$. Since routing tile is square, $S_{r,tile} = w_{r,tile}^2$. The total number of grids is calculated as $S_{chip}/S_{r,tile}$. Figure 4 shows the routing tile objects.

B. Routing Capacity Calculation

For each routing tile, there are $x$, $y$, and $z$-direction routing capacity values. $x$- and $y$-direction capacity represents available routing space on metal layers, while $z$-direction capacity is for signal TSVs. Basically, $x$- and $y$-direction capacity values of a metal layer are calculated from dividing the routing tile size by the pitch of the metal layer. Since the benchmark circuits used in this study are gate-level designs, metal layer 1 and 2 are used for local routing. Thus, we assume that only 20% of the routing capacity is available in metal layer 1 and 2. Metal 3-6 are dedicated to signal routing. In metal 7 and 8, we decrease number of routing capacity values due to the P/G nets. The capacity values based on multiple metal layer stack are added together for each tile. If the tile is pre-occupied with P/G TSVs, we decrease the capacity accordingly.

IV. Signal Interconnect for 3D ICs

We perform global routing onto $n_r \times n_r$ grid. In our routing, the thermal, power, and signal nets are routed sequentially in this order. We first route the microfluidic channels, followed by the P/G TSVs on routing tiles with no microfluidic channels. Lastly, we add P/G wires (thick and thin). The remaining area is used for signal net routing. Since the thermal and P/G interconnects are routing obstacles, we use the thermal-aware 3D maze router for obstacle avoidance under the given thermal profile [3]. After the routing is finished, we run power noise and thermal analysis to see if given constraints are satisfied. We may repeat the entire or some parts of the physical design steps with more routing area if needed.

A. Geometries of Wires and Vias

As for the signal wires, we use the metal interconnect dimensions from Intel’s 45nm technology [4]. The TSV formation approach was assumed to be via-first. In via-first approach, TSVs are formed before metal wirings are constructed. From the signal routing point of view, this is beneficial because TSVs do not touch the metal interconnection layer. By contrast, in via-last approach, a TSV passes through the entire structure and decreases the metal wire interconnection space by a large amount. TSV aspect ratio (AR, the ratio of the die thickness to the minimum TSV diameter) was assumed to be 15:1.

Fig. 3. Side view of a die layer in a stacked chip. Die is flipped and the active layer is facing down. Shapes are drawn to scale. Unit is $\mu m$. Note that signal TSVs only span single die, requiring metal layers and vias for signal TSV-to-TSV connection.
For $z$-direction capacity, we calculate the remaining surface area of each routing tile. Starting from the routing tile area, we extract the placed cell area and the P/G TSV area. Since we place P/G TSVs at the center of four routing tiles, only one quarter of P/G TSV is included in a routing tile. Then, we divide the resulting area by the minimum pitch signal TSV area. We set our routing tile size to $50 \times 50 \mu m$, which results in the following three types of routing tiles for signal net routing:

- type 1 (contains no obstacle): 618 wires for $x/y$-direction wires and 6 signal TSVs.
- type 2 (contains P/G interconnect obstacles): 371 wires for $x/y$-direction wires and 5 signal TSVs.
- type 3 (contains microfluidic channel obstacles): 618 wires for $x/y$-direction wires and 0 signal TSVs.

In case of $x$-direction interconnects, the power and thermal TSVs occupy 2.5% and 0% of the available routing area, respectively. Thus, 97.5% of $x$-direction routing resource is available for signal net routing. The same is true for $y$-direction. In case of $z$-direction, the power TSVs and the thermal interconnects (= microfluidic channels) occupy 2% and 50% of the available routing area, respectively. Thus, 48% of $x$-direction routing resource is available for signal TSVs.

V. EXPERIMENTAL RESULTS

We implemented our routing package in C++/STL and Matlab, and ran the package on a 64 bit Linux server with two AMD Dualcore Opteron 2220@2.8GHz CPUs and 16GB main memory. The circuits are from the ISPD 2006 Placement Contest benchmark that range from 200K to 1.2M gates as shown in Table I. We also show the chip size. The dimension of routing, P/G, and thermal grids is calculated from the chip size. The technology and setting parameters used in our experiments are shown in Table II.

![Routing Tile Fluidic TSV](image)

Fig. 4. Top view of routing tile. Objects are drawn to scale.

| TABLE I |
| ISPD 2006 BENCHMARK CIRCUITS. FOOTPRINT AREA IS IN $mm^2$ AND WIDTH IN $\mu m$. WE ALSO REPORT THE DIMENSIONS OF THE ROUTING, P/G, AND THERMAL GRIDS BASED ON THE CHIP AREA. |
| # cells | newblue1 | newblue2 | newblue3 | newblue4 | newblue5 |
| # nets | 221,142 | 338,901 | 552,199 | 843,128 | 1,233,058 |
| area | 36 | 56.25 | 64 | 225 | 256 |
| width | 6,000 | 7,500 | 8,000 | 15,000 | 16,000 |
| r-grid | 120x120x4 | 150x150x4 | 160x160x4 | 300x300x4 | 320x320x4 |
| p-grid | 30x30x4 | 37x37x4 | 40x40x4 | 75x75x4 | 80x80x4 |
| r-grid | 30x80x4 | 37x80x4 | 40x80x4 | 75x80x4 | 80x80x4 |

For $z$-direction capacity, we calculate the remaining surface area of each routing tile. Starting from the routing tile area, we extract the placed cell area and the P/G TSV area. Since we place P/G TSVs at the center of four routing tiles, only one quarter of P/G TSV is included in a routing tile. Then, we divide the resulting area by the minimum pitch signal TSV area. We set our routing tile size to $50 \times 50 \mu m$, which results in the following three types of routing tiles for signal net routing:

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The bottleneck was related to TSVs, since these signal TSVs compete and interfere with signal net routing. The major signal net routing distribution network for 3D IC requires a high demand on TSVs removing the hotspots in 3D designs. We also learned that the P/G liquid cooling based on micro-fluidic channels is highly effective in thermal, and P/G interconnects. Our studies revealed that the entire stack is simultaneously switching on.

Table IV shows the summary of power noise simulation results. Peak power noise values are quite high for all circuits. It was found that the maximum peak power noise location has high correlation with the maximum power consumption location. This is because we assumed the worst-case scenario in which the current profile for the entire stack is simultaneously switching on.

VI. Conclusions

In this paper, we presented the first work on routing with signal, thermal, and P/G interconnects. Our studies revealed that the liquid cooling based on micro-fluidic channels is highly effective in removing the hotspots in 3D designs. We also learned that the P/G distribution network for 3D IC requires a high demand on TSVs and interfere with signal net routing. The major signal net routing bottleneck was related to TSVs, since these signal TSVs compete with P/G TSVs and micro-fluidic channels for vertical routing resources.

Fig. 5. Routing usage of newblue5: (a) x-direction, (b) y-direction, (c) z-direction (= between die 1 and die 2). The horizontal white lines denote microfluidic channels.

Fig. 7. Peak power noise on the top layer of newblue5. Unit is V.

Table IV shows the summary of power noise simulation results. We report average and maximum peak power noise in mV.

Table IV

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Fig. 8. Waveform of the grid with maximum peak noise in newblue5.

P/G TSVs and micro-fluidic channels for vertical routing resources.

REFERENCES


