Co-design of Reliable Signal and Power Interconnects in 3D Stacked ICs

Young-Joon Lee, Mike Healy, and Sung Kyu Lim
School of Electrical and Computer Engineering
Georgia Institute of Technology, Atlanta, Georgia, U.S.A.
email: {yjlee, mbhealy, limsk}@ece.gatech.edu

Abstract—With the rapid advance of die stacking and through-silicon-via fabrication technologies, the era of 3D ICs is near. Yet, the knowledge base of 3D IC design techniques is still not matured enough. In this paper, we investigate the design issues raised during the system-level integration of signal and power interconnects in 3D ICs. Routing congestion and power noise are analyzed, and various factors that affect performance and reliability metrics are identified.

I. INTRODUCTION

One of the major challenges in 3D stacked IC is power delivery. As the fabrication technology advances, power consumption of the chip increases. According to ITRS projection, the power consumed by a single chip will reach 200W in a few years. Even in the packages of today’s industry designs, more than half of the IO pins (or C4 bumps) are dedicated for power and ground connections. As multiples chips are stacked together into a smaller footprint, delivering current to all parts of the 3D stack while meeting the noise constraints becomes highly challenging. This is mainly because the number of through-silicon-vias (TSVs) available for signal nets and P/G nets is limited, causing severe routing congestion if many 3D connections are desired. But, most of the existing studies on power delivery and signal delivery are done in isolation, thereby lacking system-level perspective. Our main contributions are as follows:

- We take a holistic approach on the reliable mechanisms of signal and power delivery. The goal is to co-design the on-chip routing geometries for signal and power interconnects in 3D stacked ICs under power noise and routability objectives.
- Several high-impact geometric configuration parameters that affect the system performance and reliability are presented and explored. We vary these parameters and demonstrate their effect on performance and reliability metrics.

II. OVERVIEW OF 3D PHYSICAL DESIGN

Our design package is divided into five steps: 1) After reading the input circuit, partitioning stage starts. In this stage, the input circuit is divided into four parts for 4-die stack implementation. We used the mincut algorithm [1] to minimize the total number of signal TSVs. 2) In the placement stage, we perform global placement of gates. 3) We perform global routing. We first route the signal nets, then P/G TSVs and P/G wires. 4) We rip up and reroute signal nets with routing capacity violations. We used the thermal-aware 3D Steiner router [2]. 5) After the routing is finished, congestion and power noise analysis is performed.

III. POWER DELIVERY NETWORK FOR 3D ICs

Our power delivery network is shown in Fig. 1. In our work, P/G TSVs are placed regularly in a mesh structure with a predefined pitch. The width of a P/G tile is a half of the power TSV pitch and contains one quarter of power TSV and one quarter of ground TSV. P/G nets are routed on metal layer 7 and 8. P/G thick wires have 10um width and runs between P/G TSVs. Between the thick wires, 40 P/G thin wires are placed. And between two P/G thin wires, several signal wires can be routed.

In our 3D technology, two signal TSVs from two adjacent dies are connected using the metal layers and local vias, i.e., two stacked signal TSVs are not directly connected (= so called via-first TSVs). On the other hand, P/G TSVs pierce through all 4 dies for efficient power delivery (= so called via-last TSVs) (see Fig. 2). Thus, no gate or decap can be placed at P/G TSV locations. Power is fed from the package through P/G I/O bumps distributed over the bottom-most die and travels to the upper dice using TSVs and solders [3]. High performance systems require dense P/G grids for both power distribution and signal current return purposes.

For a 3D chip stack structure with footprint size of 1cm², we may have thousands of P/G I/Os for each die and millions of wire segments on the P/G grids in each die. Our power noise analyzer is based on modified nodal analysis (MNA) [4]. We use domain decomposition (DD) [5] to increase the maximum circuit size the analyzer can handle. The DD technique basically decomposes the...
IV. SIGNAL INTERCONNECT FOR 3D ICs

As for the signal wires, we use the metal interconnect dimensions similar to the ones in Intel’s 45nm technology [6]. The TSV formation approach was assumed to be via-first, and a TSV aspect ratio of 10:1 was assumed. These via-first TSVs interfere with gates but not with interconnect layers (see Fig. 3). The diameter of signal TSVs is set to the minimum size to accommodate as many connections as possible. In contrast, the diameter of P/G TSVs is 40µm, which is 4x larger than that of signal TSVs. The width of a routing tile is 50µm.

For each routing tile, there are x-, y-, and z-direction routing capacity values. x- and y-direction capacity represents available routing space on metal layers, while z-direction capacity is for signal TSVs. Basically, x- and y-direction capacity values of a metal layer are calculated by dividing the routing tile size by the pitch of the metal layer. We assume that only 20% of the routing capacity is available in metal 1-2. Metal 3-6 are dedicated to signal routing. In metal 7 and 8, we decrease number of routing capacity values due to the P/G nets. Then, the capacity values of metal layers are added together for each tile. If the tile is pre-occupied with P/G TSVs, we decrease the capacity accordingly.

For z-direction capacity, we calculate the remaining surface area of each routing tile. Starting from the routing tile area, we extract the placed gate area and the P/G TSV area. Then, we divide the resulting area by the area calculated with the signal TSV pitch.

V. EXPERIMENTAL RESULTS

We implemented our design package in C++/STL and MATLAB. The simulations were done on a 64-bit Linux server with two quadcore Intel Xeon 2.5GHz CPUs and 16GB main memory. The circuit into several parts and uses a mathematical technique to reduce the time needed for matrix inversion.

Table I shows the signal and P/G interconnect routing results, where we report the average utilization of the routing tiles in x-, y-, and z-directions on die 1. We also report the number of signal TSVs for all dies.

Table II shows the signal and P/G interconnect routing results, where we report the average utilization of the routing tiles in x-, y-, and z-directions on die 1. We also report the number of signal TSVs for all dies. The run time of signal routing stage was about 10 minutes.

A. Routability and Congestion Analysis

We did the experiments with the baseline setting, i.e., Table I. Out of a single device layer, 58.26% was used for gate cells, 4.48% for signal TSVs, 2.00% for P/G TSVs, 28.61% for decaps, and 6.65% was whitespace. We calculated the unused silicon area, and assumed that 80% of the unused area is used for decap. To model simultaneous switching noise, we used an inductance of 3nH and a resistance of 3mΩ, respectively. In order to determine decap area ratio at each grid point, we calculated the used silicon area, and assumed that 80% of the unused area is used for decap. To model simultaneous switching noise, we used an inductance of 3nH and a resistance of 3mΩ, respectively. In order to determine decap area ratio at each grid point, we calculated the used silicon area, and assumed that 80% of the unused area is used for decap. To model simultaneous switching noise, we used an inductance of 3nH and a resistance of 3mΩ.

B. Power Noise Analysis

In our 3D RLC power grid, power consumption for each grid location was modeled as a current source. The gate oxide thickness was set to 1nm for decap size calculation. And the inductance and the resistance of package pins was assumed to be 0.3nH and 3mΩ, respectively. In order to determine decap area ratio at each grid point, we calculated the used silicon area, and assumed that 80% of the unused area is used for decap. To model simultaneous switching noise, it was assumed that 1/8 area of each die is turned on together with the current profile of 5nA rise time. The supply voltage was assumed to be 1V. After simulation, we gathered the peak power.
C. Varied Configurations and Their Impacts

We varied several setting parameters to investigate the impact on performance metrics: bulk Si thickness (µm) = [20, 40, 60], TSV aspect ratio = [5:1, 10:1, 15:1], P/G TSV diameter (µm) = [20, 40, 60], P/G TSV pitch (µm) = [200, 400, 600], P/G thin wire ratio = [0.2, 0.5, 0.8]. Note that the medium values were our baseline setting.

Figure 5 shows the power noise level at the grid with maximum peak noise on die 0 of baseline. Only die 0 result is shown, which showed the highest power noise level. The maximum noise level was 78.83mV.

Figure 6 shows the average routing usage with varied bulk Si thickness, TSV aspect ratio, and P/G thin wire ratio. With increased bulk Si thickness, z-direction routing usage rises quickly, because thicker die makes signal TSV diameter bigger and decreases z-direction capacity. Increasing TSV aspect ratio decreases x-direction routing usage noticeably, because signal TSV diameter gets smaller and thus z-direction capacity increases. In addition, increasing P/G TSV pitch decreased x- and y-direction routing usage due to less number of P/G TSVs that block x- and y-direction signal interconnects.

In Figure 7, maximum power noise values with varied settings are shown. Although higher TSV aspect ratio resulted in bigger decap area, the power noise got worse. In addition, bigger P/G TSV diameter was not quite helpful in decreasing power noise. The on-chip power delivery path consists of P/G I/O pins, P/G TSVs, P/G thick wires and P/G thin wires, and the parasitic values of P/G TSVs are not a dominant factor for power noise. Rather, decreasing P/G TSV pitch or increasing P/G thin wire ratio helped decrease power noise more significantly. P/G thin wires have relatively high resistance and affect voltage drop more dramatically. Thus, it is crucial for designers to carefully choose P/G TSV pitch and thin wire ratio.

Figure 8 shows the number of signal TSVs with varied settings. Varying bulk Si thickness did not change the number of signal TSVs much, because the routing congestion was not severe with the variations. The same can be said with varying P/G TSV pitch. However, lowering TSV aspect ratio and thus decreasing the z-direction capacity made the congestion problem as shown in Figure 6, and the router did not use as many signal TSVs as other settings.

VI. CONCLUSIONS

In this paper, we presented the routing results of signal and power interconnects with a 4-die 3D IC. In addition, the configuration parameters that affect system performances were identified. Understanding the interaction between signal and power interconnects is essential for optimal design.

REFERENCES