Layout-Level Synthesis of RF Inductors and Filters in LCP Substrates for Wi-Fi Applications

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Abstract—A fast and accurate layout-level synthesis and optimization technique for embedded passive RF components and circuits such as inductors and bandpass filters have been presented. The filters are composed of embedded inductors and capacitors in a multilayer liquid crystalline polymer substrate. The proposed approach is based on a combination of segmented lumped-circuit modeling, nonlinear mapping using polynomial functions, artificial neural network-based methods, and circuit-level optimization. Synthesis and optimization results of inductors for spiral/loop designs based on microstrip and stripline configuration are within 5% of data obtained from electromagnetic (EM) simulations. For RF circuits, the methodology has been verified through synthesis of 2.4- and 5.5-GHz bandpass filters with and without transmission zeros. Scalability has been shown over a range of 2–3 and 4–6 GHz, respectively, with bandwidth variation of 0.5%–3% of center frequency. The synthesized models are within 3%–5% of EM simulation data.

Index Terms—Artificial neural networks (ANNs), filter synthesis, inductor optimization, liquid crystalline polymer (LCP), synthesis.

I. INTRODUCTION

WITH THE evolutionary development in wireless communications technology, the need for low-cost, small-size, and high-performance RF front-end modules is continuously increasing. For integration, there is a clear need for design cycle time reduction of passive and active RF modules. This is important because layout level electromagnetic (EM) optimization of RF circuits has been the major bottleneck for reduced design time. Circuit simulators that use coarse circuit models are time efficient, but do not have sufficient accuracy. The focus of this paper is the development of methods that enable the synthesis of layouts for new technologies, which significantly reduces the design cycle time.

In RF designs, the physical effects of layout such as EM coupling and parasitics affect circuit performance. Furthermore, with the emergence of multiple frequency standards, the electrical specifications of components have different constraints. For example, a voltage-controlled oscillator (VCO) operating at 2.45 GHz may require an inductor with a self-resonance frequency (SRF) of at least 5.5–6 GHz with a high-quality factor (Q). However, a 5.8-GHz VCO may require an inductor with a high SRF (>8–10 GHz) and a reasonable Q. Design requirements of this kind can lead to very long EM simulation time. Since a liquid crystalline polymer (LCP) substrate provides design flexibility of RF circuits across a large frequency range (0.5–20 GHz) by embedding the passives in the substrate [1]–[5], a time-efficient design-constraint-based synthesis and optimization technique can be very useful. High-performance miniaturized filters, low-noise amplifiers (LNAs), VCOs, duplexers, and baluns functional from 500 MHz to 6 GHz using embedded inductors and capacitors on multilayer organic laminate substrate with LCP have been reported in [1]–[6]. The inductors demonstrated have Q’s varying from 30 to 200 for an inductance range of 1–25 nH [6]. The capacitors with a capacitance density of 1 pF/mm² and Q’s greater than 300 have also been demonstrated [6]. In this paper, a synthesis method has been described and applied to embedded passives in LCP substrates. The synthesized models and layouts have been compared with EM modeling results for accuracy and speed.

Optimization of silicon-based RF inductors based on geometric programming has been described in [7]. The method is limited by the use of analytical expressions for inductor parameters. This is because it is difficult to extract analytical expressions for inductor parameters on multilayer substrates. Polynomial mapping [7], [8] provides good interpolation for single or multiple parameter variations for weakly nonlinear data. However, this method does not provide convergence to a unique solution, which is optimum. Efficient EM optimization techniques using space mapping have been described in [9]–[11]. This method is ideally suited for optimizing structures once it has been generated. Artificial neural network (ANN)-based modeling techniques have also been applied for optimization of linear and nonlinear circuits [12]–[15]. However, this technique is limited by the complexity of the models for complete circuits that have multiple active and passive components. Recent research has reported the application of ANNs and aggressive space mapping (ASM) based on coarse models for design optimization of compact RF passive circuits on multilayer substrates like low-temperature co-fired ceramic (LTCC) technology [16], [17]. However, the focus of these studies is on time-efficient layout optimization and not synthesis.

This paper presents a method for the layout-level synthesis of RF passive circuits. The synthesis method has been demonstrated on a multilayered organic substrate with an LCP dielectric material (εr = 2.95, tanδ = 0.002), which is a new technology for embedding RF passive devices [1]–[4].
The method presented in this paper enables the synthesis of inductors and filters based on the constraints imposed by design specifications. The technique is based on nonlinear mapping of inductor and filter geometries and its electrical specifications using ANNs and polynomial functions with a limited EM dataset. The synthesis approach has the following advantages.

1) It enables global tradeoff analysis between competing objectives such as area, $Q$, and SRF for inductors and capacitors.
2) It uses a small dataset for neural model training by using interpolation techniques.
3) It enables inductor and circuit synthesis across various topologies.
4) It allows for the mapping between electrical response and physical parameters.
5) It enables scalability of the synthesized layout over a range of $\pm 20\%$ of center frequency (CF).
6) It allows bandwidth controllability of $0.5\%$–$5\%$ of CF.
7) It enables reduction in the number of iterations for EM simulations performed on the layout to meet design specifications.

This paper is an extension of the work on synthesis published by the same authors in [18]. This paper is organized as follows; Section II discusses the importance of synthesis in RF circuits. Section III discusses LCP technology that has been used to demonstrate synthesis. Synthesis of inductors have been discussed in Section IV. This is followed by filter synthesis in Section V. The paper finally concludes with a summary of the contributions of this work in Section VI.

II. SYNTHESIS OF RF CIRCUITS

Synthesis is the process of extracting network/layout-level parameters for a component/circuit from electrical specifications. It is common in digital designs and is being increasingly used in low-frequency analog circuits. The main reason for this is the scalability of design cells, which allows an automated hierarchical design flow. RF designs, however, lack this scalability due to the effects of layout level parasitics on circuit performance. Fig. 1 shows the steps involved in developing a synthesis method for RF circuits. A conventional design flow tries to optimize circuit performance at the layout level at the premium of time-consuming EM iterations for entire layouts. In contrast, a synthesis approach extracts physical dimensions of the layout from the electrical specifications by using some intermediate circuit-level modeling and optimization. As shown in Fig. 1, the synthesis method develops a lumped-circuit model with parasitics from a layout. In order to scale the model to a different frequency specification without multiple EM iterations, the synthesis method performs optimization at the circuit level. After optimization, the physical dimensions of the layout are extracted using polynomial functions that map the circuit geometries to their component values.

III. EMBEDDED PASSIVES IN LCP SUBSTRATE

LCP is a low-loss material ($\tan \delta = 0.002$) with a relative permittivity ($\varepsilon_r$) of 2.95. These material properties are invariant up to 20 GHz with negligible moisture absorption (0.04%). As a result, the embedded passives provide high $Q$ and stability of component values across a large frequency range [6]. The process is low cost due to the use of large area manufacturing, as shown in Fig. 2. Furthermore, the process is low temperature (200 °C) and large area (12 in × 18 in) boards can be batch fabricated, making it compatible with a printed wiring board (PWB) infrastructure. The photograph of a fabricated LCP board (size of 9 in × 12 in) containing 10,000 bandpass filters is shown in Fig. 2.

The bandpass filter is an important block in the design of an RF front-end. With the convergence of multiple frequency standards, the design of filters requires controllability of passband ripple, bandwidth, stopband attenuation, and harmonic rejection. High-performance miniaturized filters have been designed on LCP across different topologies to meet different frequency specifications, which include inductively coupled resonator filters, coupled line filters, and a capacitively coupled filter [5], [6]. Designs are also based on hybrid topologies with a combination...
of coplanar waveguide (CPW) and stripline configurations to ensure compact designs in a multilayer substrate. The filters are electromagnetically shielded with the use of top–bottom ground planes for reducing signal coupling from adjacent blocks. Fig. 3 is a photograph of fabricated filters with a size of 2 mm × 2 mm × 1.2 mm for Wi-Fi applications. The cross section used for the filters is shown in Fig. 4. It consists of a four-metal-layer stackup with top and bottom ground planes. The core dielectric material (ε_r = 3.35) on either side of the LCP layer has low loss and has a thickness of 36 mil. The laminated LCP and the metal layers are 1- and 0.5-mil thick, respectively.

The passives are designed on the middle two metal layers. The entire cross-sectional thickness of 1.8 mm (can be as low as 0.9 mm) was fixed in the designs that have been synthesized in this paper. In addition to the synthesis of filters, details on inductor synthesis have also been described. This is because, for a fixed cross section, the capacitance is a function of the width and the length and its Q value is limited by the loss tangent (tan δ) of the dielectric material [6]. However, inductors have multiple geometrical parameters such as side-length, linewidth, line spacing, and number of turns. Furthermore, inductor Q values are comparatively lower than capacitors, which make the geometry optimization during inductor synthesis an indispensable part of RF circuit design.

**IV. LAYOUT LEVEL SYNTHESIS OF INDUCTORS**

In the absence of extensive design libraries of embedded passives in LCP substrates, synthesis techniques for inductors based on design constraints is important. Methods for optimization of inductor geometries in a multivariable design environment have been addressed in [7] and [8]. In contrast, this section provides a layout-level synthesis technique for inductors used in RF front-end modules.

**A. Nonlinear Mapping Using ANNs**

In the design of inductors, a nonlinear relationship exists between electrical parameters like inductance (L), Q, and SRF and geometrical design variables such as side length, linewidth, line spacing, and number of turns. ANNs have emerged as a powerful alternative to numerical and analytical modeling techniques for capturing nonlinear circuit behavior. ANNs are preferred due to their asymptotic properties and because they give very smooth results for approximating discrete measured and simulated data. Fig. 5 shows a multilayer perceptron-based neural-network structure that has been used in this paper. During forward mapping, from the inductor geometries to the electrical parameters, the input neurons \([x_1, x_2, \ldots, x_n]\) receive the inductor geometries and the output neurons \([y_1, y_2, \ldots, y_m]\) produces \(L, \text{SRF}, \text{and } Q\) as the output, \(n\) and \(m\) being the number of inputs and outputs in a general ANN structure. The datasets get reversed during reverse mapping. A single hidden layer of neurons has been used in this paper. The outputs from all the processing units are summed through weights \((w_{ij})\) to produce \(\gamma_i\) given by (1). This output passes through the activation function given by (2) as follows:

\[
\gamma_i = \sum_{j=0}^{N_i-1} w_{ij} z_j^{-1}
\]  

\[
\sigma(\gamma) = \frac{e^\gamma - e^{-\gamma}}{e^\gamma + e^{-\gamma}}.
\]
The activation function shown in (2) is a hyperbolic tangent function. After passing through the activation function, the output dataset is obtained as shown in (3) as follows:

\[
\sigma(\gamma^L_i) = \gamma^L_i = \sum_{j=0}^{N_s-1} w_{ij} \gamma^L_j + b_{0i}. \tag{3}
\]

In this paper, Levenberg–Marquadt nonlinear optimization algorithm has been used to train the neural network, as it is an efficient method for training multilayer feedforward neural networks compared to Newton-quasi and other gradient-based training methods [19]–[21].

B. Neural-Network Training and Adaptive Data Sampling

In this paper, an initial library of 150 spiral and loop inductors [5] based on stripline and microstrip topology, respectively, were simulated using Sonnet, a commercially available two-and-one-half-dimensional (2.5-D) full-wave method-of-moments-based EM solver. The layout of an inductor in Sonnet is shown in Fig. 6. The cross section used for microstrip design is shown in Fig. 7, while the inductors with stripline topology have the cross section shown in Fig. 4. The inductance and quality factor were extracted from Sonnet data as \( L = \text{Imag}[Z_{11}]/2\Pi f \) and \( Q = \text{Imag}[Z_{11}]/\text{Re}[Z_{11}] \), while the SRF was measured at the impedance transition frequency, as shown in Fig. 8. For the training of the neural networks to “coarsely” map the input dataset to the output, 80% of the 150 inductors simulated were used. When the remaining 20% of the inductor designs were used to test the neural networks, the mapping accuracy was worse than 10%. This is because the number of data points (120) that was used for training the neurons was not sufficient to develop a mapping with the desired accuracy. The inductor \( Q \), area, \( L \), and SRF were represented as nonlinear functions of inductor side length, width, and turns, shown in (4) and (5) as follows:

\[
f = \sum_{k=1}^{M} b_{kj} \left( \sum_{i=1}^{N_s} a_{ji} x_i + a_{oj} \right) + b_{ok}. \tag{4}
\]

\[
g(x) = \frac{(e^x + e^{-x})}{(e^x - e^{-x})} \\
x = \{ \text{side length, width, turns} \}. \tag{5}
\]

where \( f \) represent \( Q, L \) and SRF; \( b \) and \( a \) are weights associated with the neural network, \( N \) represents the number of hidden neurons, \( M \) represents the number of outputs, and \( x \) is the regressor vector [19], [20]. In the design of a spiral inductor library from EM simulations, for example, the number of turns varied from 0.75 to 1.75 in steps of 0.25. For each of these designs, the side length varied from 0.5 to 3.75 mm in steps of 2.05 mm and width \( (w) \) from 0.025 to 0.225 mm in steps of 0.075 mm. The orders of magnitude of various input and output parameter values of inductors are very different. Therefore, a systematic preprocessing of training data called “scaling” is desirable for efficient neural-network training. The EM simulation data was normalized before being fed to the neural network. The data was scaled with respect to the maximum and minimum of the data range for each electrical/geometrical parameter using linear scaling, shown in (6) as follows:

\[
x_{sc} = x^0_{\text{min}} + \frac{(x - x_{\text{min}})(x^0_{\text{max}} - x^0_{\text{min}})}{(x_{\text{max}} - x_{\text{min}})}. \tag{6}
\]

Fig. 9(a)–(c) shows the variation of different electrical parameters for a section of the dataset. There is an apparent discontinuity in Fig. 9(a)–(c) when compared to the smooth contours of Figs. 10 and 11. It should be seen that in Fig. 9(a)–(c), there is no sample point in the region of discontinuity, rather sample points exist only in the smooth regions. The ANN-modeled plot for the training dataset looks the way it is because the variation of parameters were taken for different widths of the inductor geometries. Every monotonic section
Fig. 9. Forward mapping of ANN-modeled data and EM data of electrical parameters in a training subset. (a) Variation of SRF. (b) Variation of Q. (c) Variation of $L$.

of the curve represents geometry variations with respect to a single width. The next monotonic section begins with the next

Fig. 10. MATLAB TrainLM ANN model to EM data correlation in forward mapping after training of ANN. Graph 1 is the EM simulation result for test data and graph 2 is the TrainLM output for test data. X-axis is the test sample number, made continuous by interpolation. (a) and (b) represent two different training results for the same test data.

Fig. 11. $L$-contour for the inductors (length in mils; 1 mm = 40 mil).

width step in between, which is the discontinuity (where as expected, no sample points exist), where $X_{\text{min}}$ and $X$ represent the normalized and denormalized values of the input data and $X_{\text{max}}^0$ and $X_{\text{max}}^\text{min}$ represent the normalized and denormalized maximum/minimum values of the data range for
During training, the number of neurons in the hidden layers were manually adjusted so that the training error (the correlation between the neuromodeled output and training data) is neither too small (less than 2%), which hampers the generalization capability of the neuromodels, nor large (greater than 10%), which reduces mapping accuracy. As stated before, it was found that the generated dataset of inductors was too small to provide accuracy within 5% of EM simulation. Generation of EM data, which is required for training of neural networks, is computationally expensive. Initially, MATLAB’s inbuilt TrainLM neural-network tool was used to train the neural models with limited EM data for forward mapping. The EM data to MATLAB neuromodel correlation for five test data is shown in Fig. 10(a) and (b). Fig. 10(a) and (b) shows an ANN model to EM data correlation for two different training instants (with the same data). The large correlation error can be seen readily.

In order to tackle this problem, the contour of electrical parameters as a function of geometry variations was developed. As an example, the contour plots for $Q$ and $L$ as a function of dominant geometrical parameters are shown in Figs. 11 and 12. It can be seen that the surfaces are roughly monotonic in nature. This means that more data points can be generated from the existing library based on interpolation.

An adaptive sampling algorithm was included in the neural-network structure developed by the authors and was used in conjunction with the training of the neural models. Based on the desired accuracy of the required $Q$, $L$, area, and SRF ($\sim 1\%$–$5\%$), the training dataset was sampled through interpolation to generate more data points (the final size of the library can be 10–15 times the size of the library developed from EM simulation). At each stage, the neural network was trained with this larger library size than the previous stage to improve mapping accuracy. The neuromodel was then used to forward and reverse map between the electrical parameters and geometries. If the design-imposed accuracy of the component values was met, the training data interpolation was stopped.

Otherwise, the training loop was iterated using interpolated data that have smaller step size. The method works very well for monotonic data variations. The only time-consuming part was the generation of highly nonlinear data points. The neuromodels were then checked for new test case values of side lengths, linewidths, and turns for inductance calculations. The correlation with modeled and EM data was within 5%. Fig. 13 shows the correlation between ANN-modeled data using the interpolation technique and EM simulation data for forward mapping using test data. The sampling technique enabled high mapping accuracy without developing extensive EM simulation data. The nonlinear mapping approach is generic and can be applied to different inductor topologies. The flowchart for the sampling algorithm is shown in Fig. 14.

C. Synthesis and Optimization

Synthesis of inductors require reverse mapping from the electrical specifications to geometries. The neuromodeled output provided multiple solutions of geometries for a given inductance...
TABLE I
SYNTHESIS FOR A 12.5-nH (@2.4 GHz) SPIRAL INDUCTOR EXHIBITING Q, AREA, AND SRF TRADEOFFS FOR A LINE SPACING OF 0.1 mm; 1 mm = 40 mil

<table>
<thead>
<tr>
<th>TURN (MILS)</th>
<th>SIDE (MILS)</th>
<th>WIDTH (MILS)</th>
<th>Q</th>
<th>L(NH)</th>
<th>SRF (GHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.5</td>
<td>101</td>
<td>9</td>
<td>135</td>
<td>12.5</td>
<td>4.1</td>
</tr>
<tr>
<td>1.75</td>
<td>91</td>
<td>9</td>
<td>120</td>
<td>12.5</td>
<td>4.1</td>
</tr>
<tr>
<td>1.35</td>
<td>94</td>
<td>6</td>
<td>97</td>
<td>12.5</td>
<td>4.6</td>
</tr>
<tr>
<td>1.5</td>
<td>87</td>
<td>6</td>
<td>93</td>
<td>12.5</td>
<td>4.75</td>
</tr>
<tr>
<td>1</td>
<td>130</td>
<td>6</td>
<td>75</td>
<td>12.5</td>
<td>4.3</td>
</tr>
<tr>
<td>1.25</td>
<td>100</td>
<td>6</td>
<td>83</td>
<td>12.5</td>
<td>4.5</td>
</tr>
<tr>
<td>3.3</td>
<td>40</td>
<td>3</td>
<td>70</td>
<td>12.5</td>
<td>6.3</td>
</tr>
<tr>
<td>2.3</td>
<td>46</td>
<td>3</td>
<td>71</td>
<td>12.5</td>
<td>5.5</td>
</tr>
<tr>
<td>3.75</td>
<td>34</td>
<td>3</td>
<td>50</td>
<td>12.5</td>
<td>5.7</td>
</tr>
</tbody>
</table>

and different values of $Q$ and SRF. Table I illustrates this situation. From a design perspective, the synthesized inductor geometry that meets the design specifications of SRF, area, and $L$ and has the maximum $Q$ is the design that is to be selected.

Mathematically, the optimization function can be written as

$$\{\text{Area} < \text{Area}_{\text{given}}; \text{SRF} > \text{SRF}_{\text{given}}; \text{maximize}\{Q\}\}$$

where $\text{Area}_{\text{given}}$ is the maximum area of the inductor allowed by a design and $\text{SRF}_{\text{given}}$ is the minimum SRF required for the inductor in the design. The design space exploration leading to the synthesis of inductors can be formulated as follows.

Let the geometry dataset associated with the $i$th inductor be given by (8) as follows:

$$X^i = [x_1^i, x_2^i, \ldots, x_N^i]^T, \quad i = 1, 2, \ldots, M$$

where $N$ is the number of geometrical parameters and $M$ is the number of inductors. The area of the inductor ($A^i$) can be obtained as a function of $X^i$ as $A^i = \varphi(X^i)$, where $\varphi$ represents the geometrical relationship. Let the dataset for $Q$, SRF, and $L$ and $\text{Area}$ ($A$) for the $i$th inductor be given by

$$E^i = [Q^i, \text{SRF}^i, L^i, A^i]^T, \quad i = 1, 2, \ldots, M$$

The neural network described earlier has been used to develop weighted mapping functions to map $X^i$ to $E^i$ through the forward-mapping procedure and $E^i$ to $X^i$ through the reverse-mapping procedure. The algorithm for design space exploration can now be outlined as follows:

begin
initialize index, $Q_{\text{max}}$;
for $i = 1$ to $M$
   if $A^i < A_{\text{given}}$
      if $\text{SRF}^i > \text{SRF}_{\text{given}}$
         $(Q_{\text{max}} = \text{max}\{Q^i, Q_{\text{max}}\})$;
         index = $i$;
end
V. Layout-Level Filter Synthesis

Layout-level synthesis of filters in the absence of extensive design templates to meet different frequency standards can significantly reduce the time required for EM simulations and redesign. Previous work has focused on efficient optimization techniques of a pre-designed layout [9]–[11], [16], [17]. In contrast, this paper focuses on design reuse of filter layouts in LCP and enables scalability of circuit models for synthesizing layout geometries to meet different frequency specifications. The advantage lies in using a single layout template designed for a particular frequency specification and extracting layout level parameters over a range of frequencies from the same set of EM simulation data. The technique described consists of multiple levels of abstraction, which will be detailed below.

A. Development of Lumped-Circuit Models

The stages of the proposed synthesis technique at a circuit level can be best explained with the help of a circuit layout. The layout is a 3 mm $\times$ 3 mm $\times$ 1.5 mm two-pole bandpass filter at 2.45 GHz with a bandwidth of 300 MHz on an LCP substrate, as shown in Fig. 15 [22]. The layout has two inner metal layers with top and bottom ground planes (not shown in this figure), which are 1.83 mm from each other, as shown in Fig. 4. In Fig. 15, the resonator capacitors $C_{\text{resu1}}, C_{\text{resu2}}$, and $L$-resonator section $L_{\text{cp}}$ have mutual coupling, which was taken into account while segmenting the circuit. The layout was thus decomposed into circuit sections, which are isolated from each other without significant loss of accuracy [1]–[3]. In Fig. 15, the dotted lines represent the segmented sections. For example, the $L$-resonators were segmented into coupled section $L_{\text{cp}}$ and uncoupled sections $L_1$ and $L_2$. This approach allowed separate scaling and mapping of geometrical sections, which have little EM interaction between them. Based on the two- and one-port
modeling of the sections using Sonnet (which has good correlation with measurement data) [6], lumped-circuit models including the effect of parasitics and coupling were developed [6]. Fig. 15 also shows the schematic of the models for coupled L-resonator, matching capacitors $C_{m1}, C_{m2}$, center capacitor $CC$, and coupled $C_{res1}, C_{res2}$. The models showed very good correlation with EM simulation up to the second harmonic with a CF of 2.45 GHz. Due to the use of segmented models, fast optimization at the circuit level was possible to meet design specifications without losing the effects of physical layout on circuit performance.

The reference ground plane has a significant effect on the coupling between the capacitors, which affects the bandwidth characteristics of the filter. The lower plates of the two resonator capacitors were grounded through a common ground plane. During lumped-element modeling, it was seen that the mutual coupling between the two resonator capacitors is not just a function of their size and spacing, but also depends on the presence or absence of the ground planes, as shown in Fig. 16. In Fig. 16, the spacing indicates the separation between the inner edges of the top metal planes of the capacitors. Furthermore, the bottom plane has an overlay over the top plane to compensate for fringing capacitance. As a result, the bottom planes touch each other and become continuous at a point when the top planes are separated by 0.19 mm. Hence, the coupling coefficient between the capacitors in the models will have different values based on continuous or split ground planes. This effect has been included in this study through piecewise mapping.

B. Synthesis Using Model Mapping

The segmented models were made scalable based on nonlinear polynomial mapping of the circuit model parameters to EM simulation data. The one- and two-port circuit models for inductors and capacitors, taking into account the effect of coupling, were developed based on [6]. In its general form, the mapping can be mathematically outlined as follows.

Let the segmented component parameters (which include the parasitics) be represented by the vector in (10) as follows:

$$ C = [C_1, C_2, \ldots, C_N]^T $$

(10)
where $N$ is the total number of model parameters. Here, $C$ consists of all the parameters in the circuit model, which includes ideal components and their parasitics. Let us assume that for a component $C_j$, there exists a vector

$$g_i = [g_{j1}, g_{j2}, \ldots, g_{jk}]^T$$

(11)

where $k$ is the number of geometrical parameters associated with the component. Given a reference layout, its segmented components could be parameterized to generate a data set of component values with a varying geometrical parameter. This process was fast using the EM solver since it solves for sections instead of a complete layout. Let the dataset vector for a segment’s ($C_i$) $j$th geometrical parameter $g_{ij}$ be given by

$$g_{ij} = [g_{ij1}, g_{ij2}, \ldots, g_{ijn}]^T$$

(12)

where $m$ is the number of data points for which the solver was instructed to parameterize. Based on this data, nonlinear polynomial functions $\varphi_{ij}$ can be extracted for each of the geometrical sections to its corresponding component value in the model. This can be written as

$$C_i = \varphi_{ij}(g_{ij}).$$

(13)

Therefore, from the lumped-circuit model component vector

$$[C_1, C_2, \ldots, C_s]^T,$$

the geometry mapping functions can be represented by the vector

$$\left[\{\varphi_{1m}(g_{1m})\}, \{\varphi_{2m}(g_{2m})\}, \ldots, \{\varphi_{km}(g_{km})\}\right]^T$$

(14)

where each vector $\{\varphi_{jm}(g_{jm})\}$ represents all the polynomial mapped geometries (equal to $I$) associated with the component $C^s$ as follows:

$$\varphi_{ij}(g_k) = \left[\{\varphi_{i1}(g_{k1})\}, \{\varphi_{i2}(g_{k2})\}, \ldots, \{\varphi_{ip}(g_{kp})\}\right]^T$$

(15)

where $l$ is the number of geometrical parameters associated with $C^s$. The circuit level optimization parameters in the entire model is a subset of the entire model parameter $C$ and is given by (16) as follows:

$$[C_1, C_2, \ldots, C_s]^T$$

(16)

All the optimization parameters in the model now have mapping relations to its geometries given by

$$\left[\{\varphi_{1m}(g_{1m})\}, \{\varphi_{2m}(g_{2m})\}, \ldots, \{\varphi_{km}(g_{km})\}\right]^T$$

(17)

where $s$ is the number of variables selected for optimization.

The next stage is to have mapping functions, which correlates the component values to its parasitics. Let the mapping functions for this relation be given by $\phi$, where

$$C^p_i = \phi_i(C^s_i).$$

(18)

In (18), $C^p_i$ represents the parasitic associated with the component $C^s_i$ and also

$$C^s_i \cup C^p_i = C$$

(19)

where $C$ is the entire model parameter vector, as shown in (10) and $U$ represents the union of the two component sets. In conventional simulation methods, the component set $C$ is the input from which certain variables are selected for optimization. In this paper, the vector $[C^s, \phi(C^s)]^T$ is used in the optimization routine where $s$ is the number of parameters selected for optimization. At each step of the optimization of $C^s$, the parasitics also get updated through $\phi(C^s)$ in the simulation. As a result, the final optimized component values take into account the associated parasitics. Therefore, the physical effects of layout have been captured in the circuit models, while the time for simulation is reduced by performing the optimization at the circuit level. After optimization of the components in the lumped-circuit model, the geometry values could be synthesized through the reverse mapping of the same functions. Mathematically, the $j$th geometrical parameter of the $i$th component value $C^s_i$ could be extracted as follows:

$$g_{im}^* = \varphi^{-1}_{im}(C^s_{im})$$

(20)

where $g_{im}^*$ is the optimized $m$th geometrical parameter corresponding to the optimized component $C^s_{im}$. From the theory explained here, it is important to note that the reverse mapping was made under the premise that the mapping function $\varphi$ still remained the same over the frequency range in which the reference layout was scaled. This is true since the method described involves scaling of a reference layout within $+/-20\%$ of its CF with 0.5%–5% tunability in bandwidth. EM simulations over the entire frequency range of scaling have verified that the mapping functions remain unchanged. This has also been confirmed using separate reference layouts for the design of 2.4- and 5.5-GHz bandpass filters. The above methodology is best explained with the help of the layout of a bandpass filter, as shown in Fig. 15. In Fig. 15, the uncoupled inductor section in the lower half of the right lumped inductor model with shunt capacitor $C$ and series resistance $R_{12}$ were mapped to the inductor geometry as

$$L_{IP} = -0.0024(\Delta L)^3 + 0.0273(\Delta L)^2 + 0.0674(\Delta L) + 0.8104$$

(21)

$$C_{IP} = -0.0009(\Delta L)^3 + 0.0051(\Delta L)^2 - 0.0009(\Delta L) + 0.023$$

(22)

$$R_{12} = 0.0007(\Delta L)^3 + 0.111(\Delta L)^2 + 0.1082(\Delta L) + 0.0942$$

(23)

where $\Delta L$ is the increment in the inductor length of $L_1$ and $L_2$ for a fixed inductance of 0.8 nH. Similar mappings were obtained for all the circuit models. The scalable models with parasitics were combined to perform filter circuit optimization.
TABLE II
COMPARISON OF COMPONENT VALUES FOR THREE SYNTHESIS TEST CASES
BASED ON 2.45-GHZ REFERENCE LAYOUT CORRELATION OF
EM SIMULATION DATA WITH POLYNOMIAL MAPPED MODEL

<table>
<thead>
<tr>
<th>Center Freq (GHz)</th>
<th>C_m1 (pF)</th>
<th>CC (pF)</th>
<th>C_resn1 (pF)</th>
<th>L1/L2 (nH)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.45</td>
<td>Poly</td>
<td>0.50</td>
<td>0.16</td>
<td>1.80</td>
</tr>
<tr>
<td>full-wave</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2.85</td>
<td>Poly</td>
<td>0.355</td>
<td>0.065</td>
<td>1.06</td>
</tr>
<tr>
<td>full-wave</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Poly- polynomial mapping</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Full-wave – EM based data</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

using Agilent’s Advanced Design System (ADS). At each stage of the optimization process, the desired components were tuned and the corresponding polynomial-mapped geometries and parasitics were updated as well. At the end of optimization, the variable geometries of the components were extracted from the component values of the models using their reverse-mapping functions. The reverse mapping is represented by (20). As an example, the length (ΔL) and spacing (ΔS) of the inductors, as well as the width (ΔW) of the capacitors, illustrated in the previous numerical example, was reverse mapped from the component parameters as follows:

\[
\Delta L = 0.039(Lr)^3 + 0 - 982(Lr)^2 - 0.0674(Lr) + 0.6104
\]
\[
\Delta S = 0.0231(Cr)^3 + 0.051(Cr)^2 - 0.0012(Cr) + 0.032
\]
\[
\Delta W = - 0.0009(k)^3 + 0.351(k)^2 - 0.013(k) + 0.0123
\]

The values of the components obtained from synthesis and those obtained by simulating the designs in the EM solver are shown in Table II. The flowchart for the optimization and synthesis method is shown in Fig. 17.

Table II shows that the component values obtained from optimization are within 2%–5% of EM simulation using the synthesized geometries. The simulated results for the reference layout are shown in Fig. 18. Based on different design specifications, the reference layout was scaled to a design at 2.2 GHz with a bandwidth of 325 MHz and to another filter with a CF of 2.85 GHz and a bandwidth of 400 MHz. The S-parameters of the data from synthesis and that from the EM solver shows good correlation. Fig. 19 shows the EM to model correlation for a synthesized 2.2-GHz bandpass filter. Fig. 20 shows the EM to model correlation for a synthesized 2.8-GHz bandpass filter.

C. Correlation of Synthesized Model to EM Simulation

A detailed analysis of the S-parameters of the extensive lumped-circuit models and that obtained from the EM data

\[2\text{Advanced Design System 2002/doc/ccdist/SCLIN.htm} \]
D. Test Cases

The synthesis method discussed was applied to bandpass filters across frequencies and topologies. Reference layout of filters at different frequency bands and with transmission zeroes were synthesized. Synthesis results will be discussed below.

1) 5.5-GHz Bandpass Filter: The synthesis methodology was applied to a capacitively coupled resonator bandpass filter with a CF of 5.5 GHz and a bandwidth of 750 MHz. The cross section of the layout is the same as shown in Fig. 4. The filter has a lateral dimension of 2.3 mm × 2.3 mm. The layout of the filter is shown in Fig. 21. The filter has the same topology as the 2.45-GHz filter in Fig. 15. Consequently, a similar segmentation procedure was applied to the layout. For correcting the discrepancies due to via effects, which are prominent at higher frequencies, higher order mapping functions were used for the center, as well as the matching capacitors. For example, the matching capacitor $C_{rrml1}$ in the layout in Fig. 15 with parameters $Cp1, Cp2$, and $C$ were mapped to its length increment of the capacitor plates from EM simulation data by fourth-order polynomial functions as follows:

$$C_{p1} = 0.0079(W)^4 + 0.00091(W)^3 - 0.071(W)^2 - 0.069(W) + 0.0111$$

$$C_{p2} = 0.0068(W)^4 + 0.0051(W)^3 - 0.056(W)^2 - 0.041(W) + 0.031$$

$$C = 0.012(W)^4 + 0.0111(W)^3 - 0.0168(W)^2 + 0.061(W) + 0.0491.$$
TABLE III
COMPARISON OF COMPONENT VALUES FOR THREE SYNTHESIS TEST CASES BETWEEN POLYNOMIAL MAPPED MODEL AND FULL-WAVE EM SIMULATION

<table>
<thead>
<tr>
<th>Center Frequency (GHz)</th>
<th>C_{ml} (pF)</th>
<th>C_C (pF)</th>
<th>C_{res1} (pF)</th>
<th>L_{p} (nH)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.7</td>
<td>Poly 0.411</td>
<td>0.072</td>
<td>1.12</td>
<td>1.22</td>
</tr>
<tr>
<td></td>
<td>full-wave 0.393</td>
<td>0.068</td>
<td>1.15</td>
<td>1.25</td>
</tr>
<tr>
<td>5.5</td>
<td>Poly 0.350</td>
<td>0.061</td>
<td>0.98</td>
<td>0.96</td>
</tr>
<tr>
<td></td>
<td>full-wave 0.371</td>
<td>0.057</td>
<td>1.06</td>
<td>1.04</td>
</tr>
<tr>
<td>6.5</td>
<td>Poly 0.260</td>
<td>0.051</td>
<td>0.84</td>
<td>0.9</td>
</tr>
<tr>
<td></td>
<td>full-wave 0.272</td>
<td>0.050</td>
<td>0.89</td>
<td>0.95</td>
</tr>
</tbody>
</table>

Poly- data from polynomial mapping; full-wave – EM data

Fig. 23. Ideal schematic of the inductively coupled resonator filter.

Fig. 24. Layout of the 1.8-GHz filter with transmission zeros. (a) Top metal layer of the layout. (b) Bottom layer of the layout. The components have been labeled in correspondence with Fig. 23.

Fig. 25. Synthesized filters centered at 2.9 GHz from a reference layout at 1.85 GHz (EM data) based on synthesized geometries.

The synthesized model was within 2%–5% of EM simulation and similar EM modeling time as that for 2.45-GHz bandpass filter synthesis. It should be understood, however, that the segmented lumped-element technique, which was seen to work very well for two metal layer designs (considering the number of layers in which the passives are embedded) will have problems with multilayer designs (number of metal layers > 3). This was realized in modeling the inductor coupling for the filter in
and

and

and

and

represent the polynomials for mapping

represent the components of the whole

represent the map-

represent the extracted geometries for

design. The design has a lateral dimension of 6.8 mm

matching conditions and reverse mapped to obtain the dual-band

circuit model of the combined design was optimized to meet

fi

model vector for each of the two

fi

reference to (10)

dual-band

mapping functions need to be used for the two filters. With

reference to (10)–(19), such a synthesis can be mathematically

formulated, as described here. Let the entire lumped-circuit

model vector for each of the two filters be defined by \( C^1 \) and

\( C^2 \), where the vectors are similar to (10). For components for

the first filter \( C^1 \), let \( \varphi^1 \) represent the polynomials for mapping

the model parameters to geometries, and \( \varphi^2 \) represent the map-

ping of the ideal component values to their parasitics. Similar

relations hold for \( C^2 \) (in terms of \( \varphi^2 \) and \( \varphi^3 \)). Therefore, in the

circuit-level optimization of a dual-band design, the vector of

parameters that is optimized is given by (30) as follows:

\[
C_{1,2} = \left[ C_{s1}^{1,0}, \varphi^1 \left( C_{s1}^{0,0} \right) ; C_{s2}^{0,2}, \varphi^2 \left( C_{s2}^{0,2} \right) \right]^T \tag{30}
\]

where \( C_{1,2} \) represent the components of the whole filter to be

optimized and \( s1 \) and \( s2 \) are the number of components in each

filter to be optimized. The geometries for the design are ex-

tracted, as follows in (31a) and (31b), which is similar to (20)

for a single band design:

\[
g_{1,2,1}^s = \left( \varphi^1 \right)_1^{-1} \left( C_{1}^{s,0} \right) \tag{31a}
\]

\[
g_{2,1,2}^s = \left( \varphi^2 \right)_2^{-1} \left( C_{2}^{s,0} \right) \tag{31b}
\]

where \( g_{1,2,1}^s \) and \( g_{2,1,2}^s \) represent the extracted geometries for

the two bandpass filters. The filter layout of the dual-band filter

is shown in Fig. 26. The design consists of single-band filters

synthesized from the 2.45- and 5.5-GHz reference layouts. The

circuit model of the combined design was optimized to meet

matching conditions and reverse mapped to obtain the dual-band

design. The design has a lateral dimension of 6.8 mm \( \times \) 3.3 mm

with a cross section shown in Fig. 4. The EM simulation results

with the synthesized geometries are shown in Fig. 27. It consists of

two bandpass responses centered at 2.3 and 4.25 GHz with

bandwidths of 250 and 300 MHz, respectively. Synthesized de-

signs have a scalability of +/-20% of CF with a bandwidth
tenability of 0.5%–5%. This was expected since the single band

designs, from which the dual-band filter is synthesized, had simi-

lar scalability and tenability in terms of CF and bandwidth.

VI. CONCLUSIONS

This paper has presented a fast and accurate layout-level

synthesis of RF passive components and circuits in multilayered

organic substrates with LCP dielectric material. It is based on

segmented lumped-circuit modeling, polynomial mapping, and

circuit-level optimization. An optimization technique based on

ANNs and design space exploration has also been discussed

for inductor synthesis. Synthesized results for components and

circuits show accuracy that is within 5% of EM data. The ANN-

based technique was not applied in the synthesis of inductors in

the bandpass filters. This is because the inductors in the bandpass

filters were less than 2.5 nH for which simple polynomial

mapping of the segmented inductor sections gave results within

3% of EM data. Design cycle time was significantly reduced

since optimization were performed at the circuit level. Filter

synthesis was demonstrated across frequencies and topologies.
The mapping technique can be also applied to diagnostic

analysis of circuit layouts in batch processing where geometrical

variations affect circuit performance.
REFERENCES


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